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An Approach for Fault Diagnosis in Sequential Circuits

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Abstract

In this Paper, introducing the methods for designing a fault-detection experiment for sequential circuits or machines. In Sequential circuits, the fault testing and diagnosis is complicated by presence of memory. So, two distinctly different approaches were developed to solve the problem of fault detection in sequential circuits.

1. Introduction

There are two types of approaches

1. 1. Circuit –Test Approaches

In this approach, the experimenter will have a complete knowledge on the circuit realizations and each fault the can occur.

1. 2. Transition –Checking Approach

In this approach, the experimenter will have no knowledge on the circuit realization but can assume the desired transition.

Although both approaches can be applied to fault detection for sequential circuits, the circuit test approach is recommended for relatively small circuits (SSI and MSI Circuits) in which circuit is known , where as the transition –checking experiment

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is recommended for relatively large circuits (MSI and LSI circuits) in which the circuit is not known to the experimenter.

Irrespective of these two experiments, there are another class of experiments called machine identification experiments. These experiments are concerned with the problem of determining whether a given n-state machine is distinguishable from all other n-state machines. Under certain conditions, this problem is shown to be equivalent to the problem of determining whether a given machine is operating correctly or not. Finally, a procedure for designing a fault-detection checking experiment is presented.

2. Circuit –Test Approach

In this approach the experiment will have the complete knowledge on the circuit realization each fault that can occur.

In sequential circuits, fault diagnosis is the process of fault location is carried out step by step, where each step depends on the result of the diagnostic experiment at the previous step. Such a test experiment is called adaptive testing. Sequential diagnosis can be graphically represented at diagnostic tree.

In this circuit test approach the function is locate the fault of the circuit by using Edge-Point testing method.

2.1. Fault Location by edge-Pin Testing

In fault diagnosis test patterns are applied to the unit under test (UUT) step-by-step. In each step, only one output signal at the edge point of the UUT are observed and their value are compared to the expected ones. The next test pattern to be applied in adaptive testing depends on the result of previous step.

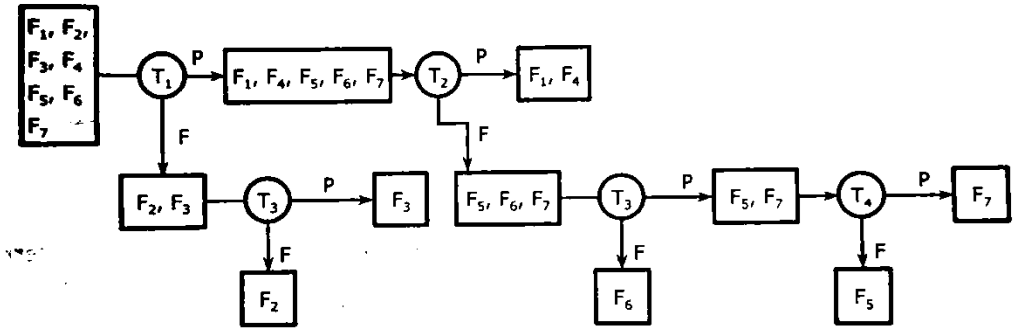

Figure 2.1 The Diagnosis Tree

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The Diagnosis tree in figure 2.1 gives the explanation for fault location using by edge –pin testing we can see that most of the faults are uniquely identified, two faults F1 F4 remain indistinguishable. Not all test patterns used in the fault table are needed. Different faults need for identifying test sequences with different lengths, the shorted test contains two patterns the longest four patterns.

Rather than applying the entire test sequence in a fixed order as in a combinational fault diagnosis, adaptive testing determines the next vector to be applied based on the result obtained by the preceding vectors. In the figure 2.1 if T1 fails, the possible faults are {F2, F3}. At this point applying T2 does not distinguish among these faults. The use of adaptive testing may substantially decrease the average number of tests required to locate a fault.

3. Transition Checking Approach

In this approach, the experimenter will not have no knowledge on the circuit realization but can assume that the desired transition. The transition –checking experiment is recommended for relatively large circuits (MSI and LSI Circuits) in which the circuit is not known to the experimenter. Figure 3.1 shows the transition –checking approach.

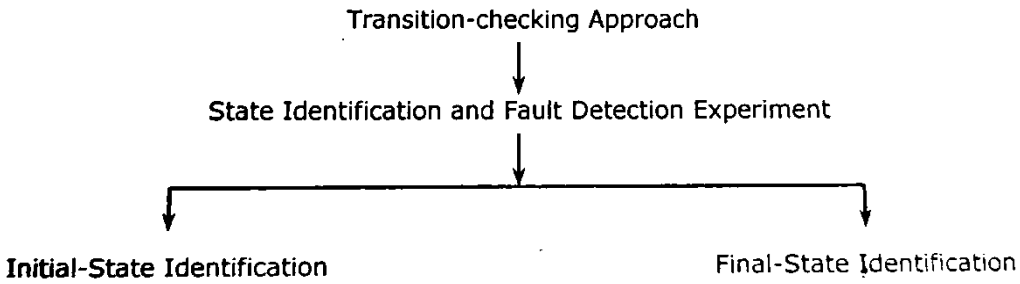

Figure 3.1 Transition Checking Approach

4. State Identification and Fault Detection Experiment

In sequential circuits, the important approach is to identity the state of the machine and then by using the state table, value we can find out the faults which are raised in the sequential circuits means state identification. State identification and fault detection of the sequential circuits are explained in two ways as,

(1) Initial –state identification

(2) Final –state identification

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4.1. Initial –state Identification

In general, the state and machine identification problems can be solved by performing a specially designed experiment on the machine. Depending on its result, we can draw our conclusion. So, first we make a precise on what we mean by an experiment.

The application of an input sequence to the input terminals of a machine is referred to as an experiment on the machine. At the beginning of an experiment, the machine is said to be in an initial or starting state and at the end of an experiment the machine is said to be in a final state.

It is customary to distinguish between two types of experiments.

(1) Simple Experiments: The experiments which are performed on a single copy of the machine

(2) Multiple Experiments: The Experiments which are performed on two or more identical copies of the machine.

In practice, most of the machines are available in just a single copy and therefore simple experiments are preferable than multiple ones.

4.1.1 Successor Tree

The root and machine identification by experiment is based on the successor tree. A successor tree is a tree-like connected graph. The procedure for constructing the successor tree of a sequential machine can be illustrated by an example.

Consider the machine M, which may initially be in any of the states A,B,C or D as given in table 4.1.

Table 4.1 Machine M1

Present State	Next State, z	
	x = 0	x = 1
A	C, 0	D, 1
B	C, 0	A, 1
C	A, 1	B, 0
D	B, 0	C, 1

The response of M1 to the input sequences 01 and 111 are listed in Table 4.2

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Table 4.2 Response of M1 to the Input Sequences of 01 and 111

(a)

Initial State	Response to 01	Final State
A	00	B
B	00	B
C	11	D
D	01	A

(b)

Initial State	Response to 111	Final State
A	110	B
B	111	C
C	011	D
D	101	A

Knowing the output sequence that M1 produces in response to the input sequence 01 is always sufficient to determine uniquely M1's final state, since each of the output sequences that might result from the application of 01 is associated with only one final state. Using the same line argument, it is evident that the output sequence that M1 produces in response to the input sequence 111 is always sufficient to determine uniquely M1's final state, as well as its initial state as given in table 4.2. Each of the output sequences that might result from application of 111 to M1 is associated with just one initial state and one final state.

Suppose a machine M, which is given to the experimenter, can initially be in any of its n state. In such case, the initial uncertainity regarding the state of the machine is given by (S1,S2….Sn). Thus, the initial uncertainity is the minimal subset of S which contains the initial state. The initial uncertainity is denoted by U0(M). The state in U0(M) are called the initial uncertainity states. Both the initial-state and final-state problems are trivial when U0(M) is a singleton (i.e, when m=1). So, we can concentrate on cases which are m>=2.

The successor tree for the machine M1 and an initial uncetainity (AB(1)) is shown in Figure 4.1

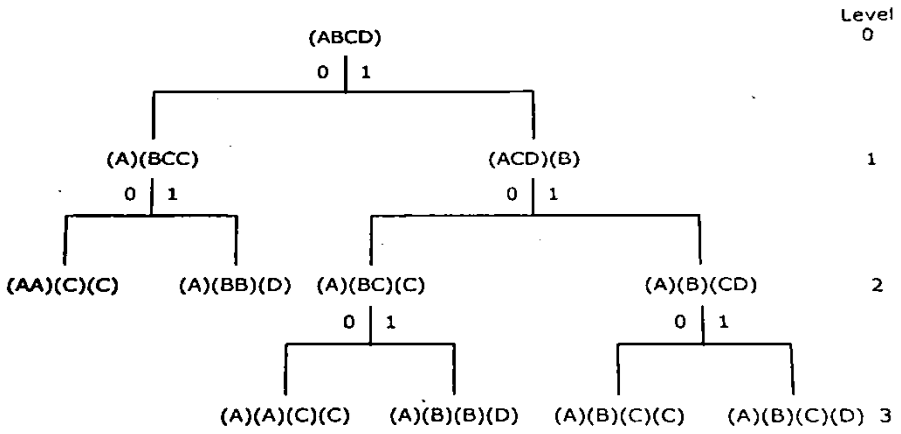

Figure 4.1 Successor Tree of M1

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In Figure 4.1, there are four levels numbered from 0 to 3. Each branch is labelled with the input symbol that it represents and every node is associated with its corresponding uncertainty vector as shown in Figure. 4.1. The highest node is associated with the initial uncertainty whereas the nodes in the level 1 are associated with its 1- and 0-successors and so on. For example, if an input symbol 1 is applied to M_1 when the U0(m) = {ABCD}, then the uncertainty vector gives (A(1))(B). If an input symbol 0 is applied, then it results (A)(BCC).

In level-1, the 1-successor of the vector (ACD)(B) is determined by obtaining the 1-successors of (A(1)) and (B) separately. For example, consider that the 1-successor of (B) is (A), then application of an input symbol 1 to M_1, when in state B, takes it to the state A. However, the 1-successor of (A(1)) will depend on the output symbol i.e., it is (CD) if the output symbol is 1 and (B) if it is 0. Thus, the corresponding uncertainty vector is (A)(B)(CD). Similarly, the 0-successor of (A(1))(B) is (A)(BC)(C), since the 0-successor of (B) is (C) while that of (A(1)) is (A)(BC).

An uncertainty is said to be smaller than another uncertainty if it contains fewer elements; e.g., (BC) is smaller than (ACD). From the way how the tree is constructed, it is evident that an uncertainty associated with a node in the j^{th} level is either smaller than or contains the same number of elements as its predecessor in the $(j-1)^{th}$ level. Suppose, in the tree of machine M_1 the successors of the uncertainty (BCC) are (AA)(C) and (A)(BB). The tree may be continued as long as it is necessary but, for it to be of practical value, a truncated version must be defined by stipulating a number of termination rules.

4.2 Final-State Identification

4.2.1 Homing Experiments

The objective for the final-state identification is to develop techniques for the construction of experiments to identify the final state of a given n-state machine. The final state of sequential machine is identified by a homing sequence, which is defined as follows,

An input sequence y_0 is said to be a homing sequence if the final state of the machine can be determined uniquely from the machine's response to y_0, regardless of the initial state.

The Homing Tree: A homing sequence for a given machine M may be obtained from a truncated version of its successor tree. A homing tree is a successor tree in which a j^{th} level node becomes terminal when either of the following occur,

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(1) The node is associated with an uncertainty vector whose non-homogeneous components are associated with some node in a preceding level.

(2) Some node in the j^{th} level is associated with a trivial or homogeneous vector.

The following tree of a machine M2 (Table 4.1) is shown in figure 4.2

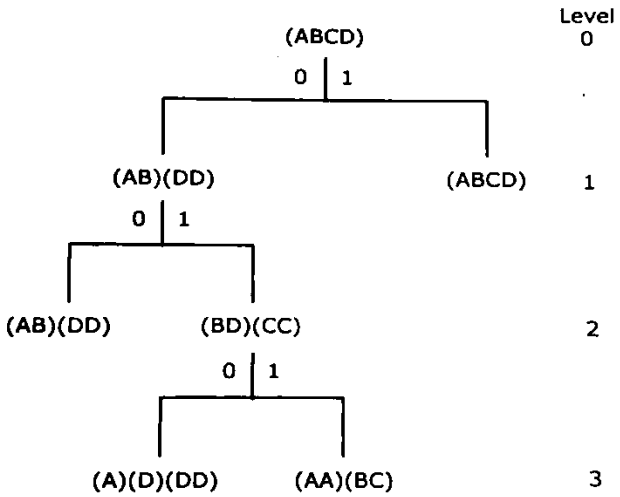

Figure 4.2 Homing Tree for M2

In Figure 4.2, the node associated with vector (AB)(DD) in level-2 is a terminal node, since its predecessor in level-1 is also associated with vector (AB)(DD). Similarly, the node (AB(1)) in level-1 is terminated, since it is identical with the node (AB(1)) in level-0. The nodes in level-3 are also terminal nodes, since (A)(D)(DD) is a homogeneous uncertainty vector. The shortest homing sequence is 010, since it is the shortest sequence described by a path leading from the 0^{th} level to a homogeneous uncertainty.

Table 4.3 Machine M2

Present State	Next State, z	
	x = 0	x = 1
A	B, 0	D, 0
B	A, 0	B, 0
C	D, 1	A, 0
D	D, 1	C, 0

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The response and final states corresponding to this sequence are given in Table 4.3.

Now, we can establish the existence of the homing sequence and derive a bound on its length using the following theorem.

Theorem 1 – A present homing sequence, whose length is at $(n-1)^2$, exists for every reduced n-state machine M.

Theorem 2 – if a synchronizing for an n-state machine M exists then its length is at most $½(n-1)^2.n$.

5. Conclusion

In this paper will give the approaches for designing a fault-detection experiment for sequential circuits or machines.

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